CLAIMS

What is claimed is:

1. A method for allowing a FIFO memory with single port memory modules to perform simultaneous read and write operations, comprising:

providing a first single port memory module for an even address of an operation;

providing a second single port memory module for an odd address of said operation;

alternating said even address and said odd address; and

when both a read request and a write request reach one of said first single port memory module and said second single port memory module at a first clock cycle, fulfilling said read request at said first clock cycle and fulfilling said write request at a second clock cycle immediately following said first clock cycle.

2. The method of claim 1, wherein said operation is selected from a group consisting of reading and writing.

3. The method of claim 1, wherein said first single port memory module and said second single port memory module are identical and are of half capacity.

4. The method of claim 3, wherein said first single port memory module and said second single port memory module are RAMs (random access memories).

5. The method of claim 4, wherein said RAMs (random access memories) are SRAMs (static random access memories).

6. The method of claim 4, wherein said RAMs (random access memories) are DRAMs (dynamic random access memories).

7. An apparatus for allowing a FIFO memory with single port memory modules to perform simultaneous read and write operations, comprising:

means for providing a first single port memory module for an even address of an operation;

means for providing a second single port memory module for an odd address of said operation;

means for alternating said even address and said odd address; and

when both a read request and a write request reach one of said first single port memory module and said second single port memory module at a first clock cycle, means for fulfilling said read request at said first clock cycle and fulfilling said write request at a second clock cycle immediately following said first clock cycle.

8. The apparatus of claim 7, wherein said operation is selected from a group consisting of reading and writing.

9. The apparatus of claim 7, wherein said first single port memory module and said second single port memory module are identical and are of half capacity.

10. The apparatus of claim 9, wherein said first single port memory module and said second single port memory module are RAMs (random access memories).

11. The apparatus of claim 10, wherein said RAMs (random access memories) are SRAMs (static random access memories).

12. The apparatus of claim 10, wherein said RAMs (random access memories) are DRAMs (dynamic random access memories).

13. A FIFO memory with single port memory modules for allowing simultaneous read and write operations, comprising:

a first single port memory module for an even address of an operation;

a second single port memory module for an odd address of said operation, wherein said even address and said odd address alternate;

a memory control module, communicatively coupled to said first single port memory module and said second single port memory module, for controlling distribution of reading and writing requests between said even address and said odd address and performance of postponed writing;

a data output selection module, communicatively coupled to said first single port memory module and said second single port memory module, for selecting a value between a first output value from said first single port memory module and a second output value from said second single port memory module and holding said value until a next read request comes;

a read and write request update module, communicatively coupled to said memory control module and said data output selection module, for updating RE (read enable) and WE (write enable) input flags to avoid reading from empty said first single port memory module and said second single port memory module and writing into full said first single port memory module and said second single port memory module; and

an address and status update module, communicatively coupled to said read and write request update module, said memory control module and said data output selection module, for updating values of address registers R_ADR (read address) and W_ADR (write address) used for access to said first single port memory module and said second single port memory module.

14. The FIFO memory of claim 13, wherein said operation is selected from a group consisting of reading and writing.

15. The FIFO memory of claim 13, wherein said first single port memory module and said second single port memory module are identical and are of half capacity.

16. The FIFO memory of claim 15, wherein said first single port memory module and said second single port memory module are RAMs (random access memories).

17. The FIFO memory of claim 13, wherein said memory control module uses a least significant bit in said address register R_ADR to indicate which of said first single port memory module and said second single port memory module is to perform a current reading request, and uses a least significant bit in said address register W_ADR to indicate which of said first single port memory module and said second single port memory module is to perform a current writing request.

18. The FIFO memory of claim 13, wherein when both a read request and a write request reach one of said first single port memory module and said second single port memory module at a first clock cycle, said read request is fulfilled at said first clock cycle and said write request is fulfilled at a second clock cycle immediately following said first clock cycle.

19. The FIFO memory of claim 13, wherein when mem_capacity is a power of 2, adr_width = log mem_capacity (on base 2), and RA = WA, FULL and EMPTY flags of said address and status update module are determined as follows: (a) when R_carry = W_carry, then EMPTY = 1; (b) otherwise, FULL = 1.

20. The FIFO memory of claim 13, wherein when mem_capacity is not a power of 2 and R_ADR = W_ADR, FULL and EMPTY flags of said address and status update module are determined as follows: (a) when ind = 1, then FULL = 1; (b) when ind = 0, then EMPTY = 1.

21. The FIFO memory of claim 13, further comprising a counter module for outputting count_width most significant bits of said counter module.